What is claimed is:

1. A semiconductor device, comprising: a plurality of wiring layers that are laminated with each other,

each of said wiring layers includes:

an interlayer insulating film;

first and second electrodes buried in the interlayer insulating film and remote from each other;

a first via that connects said first electrode and said first electrode of the wiring layer, which is provided on its upper layer or lower layer, to each other; and

a second via that connects said second electrode and said second electrode of the wiring layer, which is provided on its upper layer or lower layer, to each other, and said first electrode and said first via are connected to a first terminal, said second electrode and said second via are connected to a second terminal, and a capacitor is formed between said first electrode and said first via, and said second electrode and said second via.

2. The semiconductor device according to Claim 1, wherein a plurality of said wiring layers are provided in a same design rule with each other.

3. The semiconductor device according to Claim 1, wherein said wiring layers are provided in three or more layers.

4. The semiconductor device according to Claim 3, wherein a plurality of said first via are arranged in a position where the via overlap with each other and a plurality of said second via are arranged in a position

where the via overlap with each other, viewing from the lamination direction of said wiring layers.

5. The semiconductor device according to Claim 1, wherein a plurality of said first electrodes are arranged in a position where the electrodes overlap with each other and a plurality of said second electrodes are arranged in a position where the electrodes overlap with each other, viewing from the lamination direction of said wiring layers.

6. The semiconductor device according to Claim 1, wherein the distance between said first electrode and said second electrode is 0.3μm or less in a same wiring layer.

7. The semiconductor device according to Claim 1, wherein the distance between said first electrode and said second electrode in a same wiring layer is the minimum value that is allowed by the design rule of said wiring layer.

8. The semiconductor device according to Claim 1, wherein the distance between said first via and said second via that is formed in the closest position to the first via is the minimum value that is allowed by the design rule of said wiring layer.

9. The semiconductor device according to Claim 1, wherein said first and second electrodes are in strip shapes that are parallel to each other.

10. The semiconductor device according to Claim 9, wherein the width of said first and second electrodes is 0.3 μm or less.

11. The semiconductor device according to Claim 9, wherein the width of said first and second electrodes is the

minimum value allowed by the design rule of said wiring layers.

12. The semiconductor device according to Claim 9, wherein said first and second electrodes are provided in each of said wiring layers in plural numbers, and said first and second electrodes are arrayed alternately in each wiring layer.

13. The semiconductor device according to Claim 9, wherein regarding each of said first and second electrodes, said first and second via are provided in plural numbers by being arrayed in the longitudinal direction of said first and second electrodes.

14. The semiconductor device according to Claim 13, wherein the distance between said first via in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers.

15. The semiconductor device according to Claim 9, wherein at least one of said first and second via is a slit-shaped via extending in the longitudinal direction of said first and second electrodes.

16. The semiconductor device according to Claim 1, further comprising an integrated circuit section, wherein

the diameter of said first and second via are larger than the diameter of the via provided in said integrated circuit section.

17. The semiconductor device according to Claim 1, wherein said first terminal is connected to ground wiring, said second terminal is connected to power source wiring, and said capacitor is a decoupling capacitor connected to a power source in parallel.

18. The semiconductor device according to Claim 17, wherein said wiring layers are formed in a semiconductor chip, and said ground wiring and said power source wiring are arranged in the periphery of said semiconductor chip.

19. The semiconductor device according to Claim 1, further comprising:

an upper electrode provided in a region including a region immediately under said first and second electrodes, and connected to one of said first and second terminals;

an insulating film provided under the upper electrode; and

a lower electrode provided under the insulating film and connected to the other one of said first and second terminals, wherein another capacitor is formed between said upper electrode and said lower electrode.

20. The semiconductor device according to Claim 1, further comprising:

an N-type semiconductor layer, which is provided in a region including a region immediately under said first and second electrodes and connected to one terminal out of said

first and second terminals, to which higher potential is applied; and

a P-type semiconductor layer, which is provided in a region including the region immediately under the electrodes so as to contact said N-type semiconductor layer and connected to one terminal out of said first and second terminals, to which lower potential is applied, wherein

still another capacitor is formed between said N-type semiconductor layer and said P-type semiconductor layer.

21. The semiconductor device according to Claim 1, further comprising a semiconductor substrate provided under said wiring layers, wherein the semiconductor substrate includes:

an N-type semiconductor region, which is provided in a region including a region immediately under said first and second electrodes and connected to one terminal out of said first and second terminals, to which higher potential is applied; and

a P-type semiconductor region, which is provided in a region including the region immediately under the electrodes so as to contact said N-type semiconductor region and connected to one terminal out of said first and second terminals, to which lower potential is applied, and still another capacitor is formed between said N-type semiconductor region and said P-type semiconductor region.